REMARKS

This application has been reviewed in light of the Office Action dated July 20, 2004. Claims 51-57 are presented for examination. Favorable reconsideration is requested.

Claims 51, 53 and 56 were rejected under 35 U.S.C. 102(b) as being anticipated by UK Patent Application GB 2 204 174 A, to Seiko Instruments Inc. (Seiko). Claims 51, 55 and 56 were rejected under 35 U.S.C. 102(b) as being anticipated by JP05-241526 (Victor). Further, Claims 52 and 54 were rejected under 35 U.S.C. 103(a) as being unpatentable over Victor in view of JP02-4004 (Hitachi), and Claim 57 was rejected under 35 U.S.C. 103(a) as being unpatentable over Victor in view of U.S. Patent 6,300,922 (Teggtatz).

Claim 51 is directed to an image forming apparatus comprising: a display panel (1) adapted to display an image, and a pulse width modulation signal generator (6) adapted to input digital data corresponding to the image and a clock signal, and to count pulses of the clock signal in correspondence with the digital data to generate a pulse width modulation signal (PWMout) for driving the display panel. The pulse width modulation signal has a pulse width that corresponds to a number of pulses of the clock signal corresponding to a gray scale level of the image, and a clock generator (Figs. 31 and 36) is adapted to generate the clock signal. The clock generator is provided with a memory (203 in Fig. 31, 212 in Fig. 36) for storing a plurality of items of data and generates each pulse

of the clock signal in accordance with one (e.g., as shown in Fig. 32) of the items of data read from the memory in synchronism with a reference clock signal (nPCLK).

According to an aspect of the present invention to which Claim 51 relates, since the memory stores a plurality of items of data, a user (or the image forming apparatus per se) can select a suitable one of items of the data. The pulse width modulation signal generator inputs digital data corresponding to the image and a clock signal and counts pulses of the clock signal in correspondence with the digital data to generate a pulse width modulation signal (PWMout) corresponding to the digital data representing the image. Consequently, an image can be provided with an image quality in correspondence with a user's preference or an environment in which the image forming apparatus is set.

Seiko discloses a gray scale controller 73 for outputting a gray scale pulse in accordance with an input signal from a latch 72 and a second gray scale control clock (CLK2) from a gray scale control clock circuit 79 (as shown in Fig. 9). The second gray scale control clock (CLK2) determines the width of a gray scale pulse and generated by using a 16-bit parallel input shift register 90, to which the parallel input data determined by a relation between the reflectivity of a display panel 75 and the effective voltage is supplied, in synchronism with a clock signal (CLK).

However, Seiko does not teach or suggest generating a clock signal for a pulse width modulation in accordance with data read from a memory storing a plurality of items of the data. In Seiko, since the parallel input data is the sole item of data, the gray scale control clock circuit 79 does not generate a plurality of items of the gray scale control

clock selectively, but also the sole predetermined gray scale control clock. Accordingly, Seiko does not select an image quality in correspondence with a user's preference or an environment.

Accordingly, Claim 51 is believed to be clearly patentable over Seiko.

Victor (JP05-241526) discloses a display unit utilizing an optical element array. In Victor, a counter 8 counts a reference signal C1 from a reference signal generating means 42, and a comparator 12 compares the output of the counter 8 with digital image data from a latch 10, and the result of the comparison becomes a pulse width modulation signal of the image data. However, Victor fails to disclose a clock generator as in Claim 51, provided with a memory for storing a plurality of items of data and generating each pulse of the clock signal in accordance with one of the items of data read from the memory in synchronism with a reference clock signal.

The Office Action apparently asserts that the reference signal generating means 42 (clock generator) of Victor includes a memory ROM (paragraphs [0016] and [0021]) and changes a frequency of the reference signal C1. However, the ROM is seen merely to store properties of light modulation of an optical-light-transforming device, and the contents of the ROM are not read in synchronism with a reference clock signal.

Therefore, Victor does not teach or suggest storing a plurality of items of data in the ROM and generating each pulse of reference signal C1 in accordance with one of the items of data read from the ROM in synchronism with a reference clock signal, let alone a clock signal generator as recited in Claim 51.

Accordingly, it is respectfully submitted that Claim 51 is clearly patentable over Victor.

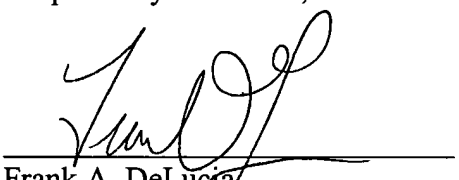
A review of the other art of record has failed to reveal anything which, in Applicant's view, would remedy the deficiencies of the art discussed above as references against independent Claim 51 herein. Accordingly, that claim is believed to be patentable over the art of record.

The other claims in this application are each dependent on Claim 51, and also are believed to be patentable over that art, at least because each depends from a patentable base claim. Nonetheless, because each dependent claim defines an additional aspect of the invention, individual reconsideration of each on its own merits is respectfully requested.

In view of the foregoing remarks, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

Applicant's undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,



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